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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,233	08/08/2001	Kerry Bernstein	BUR920010042	9886
5409	7590	03/22/2005	EXAMINER	
ARLEN L. OLSEN SCHMEISER, OLSEN & WATTS 3 LEAR JET LANE SUITE 201 LATHAM, NY 12110			ABRAHAM, ESAW T	
			ART UNIT	PAPER NUMBER
			2133	
DATE MAILED: 03/22/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.

09/682,233

Applicant(s)

BERNSTEIN ET AL.

Examiner

Esaw T Abraham

Art Unit

2133

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED on 03/08/05 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ they raise the issue of new matter (see Note below);
(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: 1-34.

Claim(s) withdrawn from consideration: _____

8. ☐ The drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Esaw Abraham

Continuation of 5. does NOT place the application in condition for allowance because: As for the argument that no power supplies are connected to the logic circuits or flip-flops in Tsukamoto et al's art, there is no logic circuit or flip-flop that operates with out power application from a common or multiple power supplies. Although the examiner strongly disagrees with the argument based on the fact that the power distribution block (19) supplies power directly or indirectly to the logic circuits, even with the absence of it, it is obvious that the prior art logic circuits cannot properly function with out being powered by power supply means.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the examiner has argued the obviousness to combine Rajassamy with the teachings of Tsukamoto et al. since Rajassamy teach all the subject matter claimed in claims 1 and 6 but does not teach power rails applied separately to each of IC chips comprise latches and logic circuits. Tsukamoto et al. in figure 4 teach a testing system comprises a burn-in board (11) to be diagnosed, a control signal generator (12) includes clock generator (12a) generates a clock signal CLK, and supplies the clock signal CLK to the burn-in board via scan signal distributor (12b), a power distributor (13) for supplying electric power Vcc to the burn-in board and in figure 5 the burn-in board shows products (IC11/IC12/IC1n, IC21/IC22/IC2n...) of a semiconductor integrated circuit device on the most common means known to one ordinary skill in the art the time the invention was made to implement the teachings of Radjassamy. One ordinary skill in the art at the time the invention was made would have been motivated in order to diagnosis the products on the burn-in board without undesirable influence of a partially defective product and automatically classifies the products between the excellent group, the partially defective group an the defective group (see col. 9, lines 48-58).

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03/14/05